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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,557	07/24/2003	Shigeo Kigo	P23981	8098

7055 7590 07/19/2007

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EXAMINER	
BECK, ALEXANDER S	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
07/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/625,557	KIGO ET AL.	
	Examiner	Art Unit	
	Alexander S. Beck	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 27, 2007 has been entered. Claims 14-25 are currently pending in U.S. Patent Application No. 10/625,557 and an Office action on the merits follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 14-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,654,728 to Kanazawa et al. (hereinafter "Kanazawa") in view of IEEE Publication "Resonant Snubber-Based Soft-Switching Inverters for Electric Propulsion Drives" by Jih-Sheng Lai (hereinafter "Lai").

As to claim 14, Kanazawa discloses a driving circuit in Figure 4 that drives a display panel having an electrode (Y1), comprising: a first switching element (SW14) that supplies a charge from a recovering capacitor (C2) to the electrode (Y1) of the display panel; and an interconnector (e.g. where inductive element L2 connects with diodes D14 and D15) connected to the first switching element (SW14) through a first one-way conductive element (D14). (Kanazawa at col. 7, ll. 31-55.) The driving circuit includes: a second switching element (SW15) that recovers the charge from the electrode (Y1) of the display panel to said recovering capacitor (C2); and a second one-way conductive element (D15) provided between said second switching element (SW15) and said interconnector. (Kanazawa at col. 7, ll. 59-67.)

A frequency reducer (e.g. positive diodes connected reversely and in parallel between the drains and sources of the switches/transistors SW14 and SW15) is connected in parallel with said first switching element (SW14), that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element (SW14), and the inductance component (L2) of the interconnector, wherein the charge is supplied to the electrode (Y1) of the display panel from said recovering capacitor (C2) through said first switching element (SW14) and said interconnector. While Kanazawa does not disclose expressly wherein

the diodes connected reversely and in parallel between the drains and sources of switches SW14 and SW15 are frequency reducers, it is well within the knowledge and skills of those of ordinary skill in the art that the diodes possess such properties as capacitances; and if added to the parasitic capacitances of the switches, the resonance frequency resulting from the parasitic capacitance of the switches would be reduced.

Kanazawa does not disclose expressly wherein the frequency reducer has a capacitance of approximately five to ten times as much as that of the parasitic capacitance of the first switching element, or wherein the frequency reducers connected in parallel with the switches are capacitors.

Lai, which is reasonably pertinent to the particular problem with which the inventor was concerned (e.g. avoiding EMI interference in a driving circuit caused by other components) and therefore analogous in art, discloses a driver circuit in Figure 3. The driving circuit is similar to that of Kanazawa, wherein in addition to the diodes connected in parallel to the switches, capacitors (Cr) are also connected to the switches in parallel as lossless snubbers in order to allow a zero-voltage turn-off and to slow the voltage rise rate (dv/dt). (Lai at p. 75 regarding *Mode 2*.)

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Kanazawa by including capacitors connected to the switches in parallel, as taught/suggested by Lai. The suggestion/motivation for doing so would have been to reduce losses during turn-off and improve the voltage rate by slowing it down. As would have been well known to those of ordinary skill in the art, introducing the capacitors into the switching circuit as taught/suggested by Lai would reduce the parasitic resonant frequency or

the "ringing" of the switching circuit because the slower voltage rise rate would inevitably lead to reducing or eliminating of such oscillation.

The examiner takes Official notice that it is old and well known in the display art to modify the parameters of electronic components during the course of routine optimization/experimentation. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Kanazawa and Lai such that the capacitive frequency reducers had a capacitance of approximately five to ten times as much as that of the parasitic capacitance of the first switching element. The rationale is as follows:

One of ordinary skill in the art would have been motivated to have had the capacitive frequency reducers with a capacitance of approximately five to ten times as much as that of the parasitic capacitance of the first switching element since such a range, absent any criticality (i.e. unobvious and/or unexpected result(s)), is generally achievable through routine optimization/experimentation, and since discovering the optimum or workable ranges, where the general conditions of a claim are disclosed in the prior art, involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955). Moreover, in the absence of any criticality, the parameters set forth above would have been obvious to a person having ordinary skill in the art at the time the invention was made. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 15, Kanazawa discloses a frequency reducer connected in parallel with the second switching element (SW15), that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said first switching element (SW14), and an inductance component (L2) of said interconnector, wherein the charge is supplied to the

electrode (Y1) of the display panel from said recovering capacitor (C2) through said first switching element (SW14) and said interconnector. While Kanazawa does not disclose expressly wherein the diodes connected reversely and in parallel between the drains and sources of switches SW14 and SW15 are frequency reducers, it is well within the knowledge and skills of those of ordinary skill in the art that the diodes possess such properties as capacitances; and if added to the parasitic capacitances of the switches, the resonance frequency resulting from the parasitic capacitance of the switches would be reduced.

As to claims 23-25, Kanazawa discloses a display device incorporating a driver, as presented in claims 14 and 15. As such, claims 23-25 are rejected on the same grounds.

As to claims 16-22, all of the claim limitations have been discussed and met by Kanazawa and Lai as detailed in the above paragraphs with respect to claims 14, 15 and 23-25.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander S. Beck whose telephone number is (571) 272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander S. Beck
July 6, 2007

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER